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Description

FIELD OF INVENTION

Present invention relates to recording systems using partial-response signaling, e.g. magnetic disk storage systems or optical disk storage systems using partial-response signaling with maximum-likelihood sequence detection (PRML). The invention relates in particular to a method for updating the tap coefficients of an equalizer in such systems, allowing to compensate the effect of channel characteristic variations with track radius, and further to an equalizer for executing this method.

BACKGROUND

In disk storage devices using partial-response (PR) signaling, a receive filter in the readback apparatus has to shape the output signal of the recording channel into a PR signal before a detection device, e.g. a maximum-likelihood sequence detector can reconstruct the recorded data sequence. However, since the recording density of data on a track, and thus the recording channel characteristic varies with track radius, a fixed filter can only shape the channel output signal into a nominal PR signal at a given track; at other radii, the spectrum of the filter output signal deviates from the nominal PR characteristic leading to a degradation in error-rate performance of the recording system. Such a loss in performance can be avoided if an adaptive equalizer is used besides the fixed receive filter, to compensate for variations in channel characteristics with track radius.

Various equalization circuits and methods for improving the operability and effectiveness of recording or communication systems are known in the art.

In the publication "Improvement of recording density by means of a cosine equalizer" by T.Kameyama et al., IEEE Transactions on Magnetics, Vol.MAG-12, No.6 (Nov.1976), pp.746-748, an equalizer was disclosed which improves the recording density in a peak detection magnetic recording system by pulse slimming. The equalizer consists of a delay line, an amplitude divider and a differential amplifier. However, the equalizer is not adaptively updated during reading data from the disk and thus cannot compensate channel characteristic variations.

An article by D.D.Falconer et al. entitled "Application of fast Kalman estimation to adaptive equalization", published in the IEEE Transactions on Communications, Vol.COM-26, No.10 (Oct.1978), pp.1439-1446, suggested to employ, for the setting of tap coefficients in an adaptive equalizer in data communication systems, a recursive least squares algorithm. This algorithm leads to rapid initial convergence of the equalizer tap coefficients. However, the algorithm requires a great number of multiplications and thus is not suited for high-speed implementation.

U.S.Patent 4,580,176 entitled "Adaptive equalization circuit for magnetic recording channels utilizing signal timing", and the article "Adaptive symmetrical interference equalization" by R.C.Schneider et al., IBM Technical Disclosure Bulletin Vol.28, No.11 (April 1986), pp.4857-4858, disclose adaptive equalizer circuits for magnetic recording systems. However, they are designed for peak detection systems and thus are not suited for recording systems using partial-response signaling.

U.S.Patent 4,041,418, entitled "Equalizer for Partial Response Signals", discloses an equalizer for correcting distorted partial-response signals that comprises a delay line and a number of taps from that delay line. The tap signals are amplified, which can be seen as multiplication with variable coefficients, and then added in an adder. Though this solution may provide a reasonably quick response for the telephone line application given as example, it is nevertheless neither suitable nor fast enough for today's rapid storage applications using partial-response signalling.

OBJECTS OF THE INVENTION

It is a primary object of the invention to compensate channel characteristic variations with track radius in recording systems using partial-response signaling.

It is a further object of this invention to devise a tap coefficient adjustment method for an equalizer of a recording system using partial-response signaling, by which the effect of channel characteristic variations with track radius is minimized.

Another object of the invention is to devise circuitry for the adaptive adjustment of the equalizer tap coefficients which is well suited for high-speed implementation.

A further object is a method of equalizer tap coefficient adjustment which enables a fast start-up of the equalizer circuitry in recording systems using partial-response signaling.

SUMMARY OF THE INVENTION

These objects are achieved by a method for tap coefficient adjustment in an equalizer of a recording system using partial-response signaling, as defined in Claim 1 and Claim 6, and by equalizer apparatus for executing this method as defined in Claim 7.

The invention compensates the effects of varying channel characteristics due to varying radius in recording systems using PR signaling, and allows fast initial adjustment (during training sequence reception) and reliable updating (during data reception) of the equalizer coefficients. Since only logic operations and no multiplications are necessary to update the tap coefficients, the equalizer is well suited for high-speed implementation.

Further features and advantages of the invention will become apparent from the following detailed description of a preferred embodiment in connection with the accompanying drawings.

LIST OF DRAWINGS

Fig.1 is a schematic overview of a PRML recording system with an adaptive cosine equalizer (ACE);
Fig.2 is a basic block diagram of the cosine equalizer;
Fig.3 is a diagram giving amplitude spectra of the cosine equalizer and of the ideal reference equalizer.
Fig.4 is a block diagram of the adaptive cosine equalizer with tap coefficient adjustment circuitry according to the invention;
Fig.5 is a block diagram of a digital implementation of the basic cosine equalizer; and
Fig.6 is a block diagram of a digital implementation of the tap coefficient gradient ($\Delta K_n/2$) computation.

DETAILED DESCRIPTION

1. PRML System with ACE

In the following, an embodiment of the invention is described for the example of a disk storage system having the following characteristics: It is a magnetic recording system using partial-response class-IV signaling with maximum-likelihood sequence detection (PRML).

A PRML system with an adaptive cosine equalizer (ACE) is shown in Figure 1. A binary data sequence $\{a_n = \pm 1\}$ is sent at the signaling rate 1/T through a magnetic-disk storage system 11, band-limiting receive filter 13, and variable gain amplifier (VGA) 15 with gain γ. The output of VGA 15 is sampled by sampling means 17, e.g. an analog-to-digital converter, at times $nT + \tau$ and the resulting samples x_n appearing on line 19 are processed by ACE 21. ACE 21 is a symmetric 3-tap digital equalizer with a center-tap value set to one. The other two taps are adjustable and have the same value K. The ACE will be described in more detail later. VGA 15 and ACE 21 together constitute a 3-tap transversal filter with coefficients γK, γ, and γK. The output samples y_n appearing on the output lines 23 of the ACE are processed by Viterbi decoder 25 to reconstruct the recorded data sequence.

For a PR-IV signaling scheme,

$$y_n = z_n + w_n , \quad (1)$$

where

$$z_n = a_n - a_{n-2} \quad (2)$$

represents the signal part and w_n is filtered noise. The fixed receive filter can shape the output of the magnetic-disk channel into the form described by (1) and (2) only at a given track radius. By adjusting the gain γ and ACE coefficient K, this form can be closely approximated at other track radii.

The effectiveness of the ACE to compensate variations of the magnetic-disk channel characteristics with track radius will be shown using a model of these variations derived from measurements. Following this model, the overall transfer characteristic of the magnetic-disk channel and receive filter is given by

$$C(f) = \eta\, C_0(f)\, e^{\Delta/2}\, e^{-2T\Delta|f|} , \quad (3)$$

where

$$C_0(f) = \begin{cases} T\left[1 - e^{-j4\pi fT}\right] & \text{for} \quad |f| < 1/2T \\ 0 \quad \text{otherwise} , \end{cases} \quad (4)$$

is the transfer characteristic of a PR-IV system. In (3), the gain parameter η and the distortion parameter Δ

model deviations from the PR-IV transfer characteristic caused by variations of the magnetic-disk channel characteristics with track radius. The term $e^{\Delta/2}$ in (3) normalizes the transfer characteristic C(f) so that at f = 1/4T, C(1/4T) = η2T is independent of the distortion parameter Δ.

2. *Cosine Equalizer*

A block diagram of a cosine equalizer is shown in Figure 2. It comprises a delay line having two delay elements 27, 29 and three taps 31, 33, 35. The sample of the center tap and modified samples of the two outer taps, each of them weighted with tap coefficient K, are combined in an adder 37 to form output sample y_n. The output sample y_n is given by

$$y_n(K) = \tilde{x}_n + K u_n , \quad (5)$$

where

$$\tilde{x}_n = x_{n-1} \quad (6)$$

denotes the sample at the center of the delay line and

$$u_n = \tilde{x}_{n+1} + \tilde{x}_{n-1} . \quad (7)$$

The filter described by (5) and (7) with $\tilde{x}_n$ as input has no phase shift; its transfer function is

$$H(f) = 1 + 2K \cos(2\pi fT) . \quad (8)$$

The transfer function of a reference equalizer that exactly compensates variations in channel characteristics for the model described by (3) and (4) is given by

$$H_0(f) = e^{-\Delta/2} e^{2T\Delta|f|} . \quad (9)$$

In Figure 3, the amplitude spectrum $|H(f)|$ of the cosine equalizer is compared to $|H_0(f)|$ of this reference equalizer for three distortion parameters Δ. The value of the VGA gain γ is chosen such that $\eta\gamma = 1$ and the coefficient K is selected to minimize the mean-squared error at the input of the Viterbi decoder. The discrepancy between $|H(f)|$ and $|H_0(f)|$ at DC and the Nyquist frequency does not result in a large mean-squared error since PR-IV signaling leads to spectral nulls at these frequencies.

3. *Tap Adjustment Procedure*

The tap adjustment scheme is derived from the fast recursive least squares (RLS) algorithm for the estimation of the optimal tap coefficient (as descibed in the paper by Falconer et al. mentioned above). At time n + 1 the tap coefficient K_{n+1}^{RLS} obtained by the RLS method is the tap value K that minimizes the cumulative squared error

$$\sum_{m=0}^{n} e_m^2(K) , \quad (10)$$

where

$$e_m(K) = y_m(K) - \hat{z}_m \quad (11)$$

represents the error signal at the output of the cosine equalizer with tap coefficient K and $\hat{z}_m$ denotes a reconstruction of z_m (see (2)) made by the receiver. The tap coefficient K_{n+1}^{RLS} can be generated recursively as follows (RLS algorithm):

$$K_{n+1}^{RLS} = K_n^{RLS} - \xi_n e_n(K_n^{RLS}) u_n \quad (12)$$

$$K_0 = 0 , \quad (13)$$

where

$$\xi_n = \frac{1}{\sum_{m=0}^{n} u_m^2} \quad (14)$$

is a time varying loop gain.

The signal sample z_n (2) can only have the values 0, ±2 and (1) suggests to reconstruct the three-level sample

$$\hat{z}_n = \begin{cases} 2 & \text{for} \quad 1 \le y_n \\ 0 & \text{for} \quad -1 < y_n < 1 \\ -2 & \text{for} \quad y_n \le -1 \end{cases} . \tag{15}$$

The term $e_n u_n$ in (12) is recognized as the stochastic gradient $1/2\, de_n^2(K_n)/dK_n$ of the mean squared error $E[e_n^2(K_n)]$ with respect to the tap coefficient K_n. Computation of this gradient requires a multiplication that can be avoided by using, according to the invention, instead of u_n the three-level reconstruction

$$\hat{u}_n = \begin{cases} 2 & \text{for} \quad 1 \le u_n \\ 0 & \text{for} \quad -1 < u_n < 1 \\ -2 & \text{for} \quad u_n \le -1 \end{cases} . \tag{16}$$

This approximation is justified by noticing that when the signal at the output of the receive filter has already the PR-IV format, leading to K = 0, then (see (1), (2), (5), and (7))

$$u_n = y_{n+1} + y_{n-1} = a_{n+1} - a_{n-3} + w_{n+1} + w_{n-1} = \begin{cases} 2 + \text{noise} \\ 0 + \text{noise} \\ -2 + \text{noise} \end{cases} . \tag{17}$$

An approximate tap gradient can now be computed without multiplication. It is advantageous to compute the sum of two consecutive gradients in order to reduce variance. This leads to

$$\Delta K_n = e_n(K_n)\,\hat{u}_n + e_{n-1}(K_{n-1})\,\hat{u}_{n-1} . \tag{18}$$

This gradient is used to update the tap coefficient by:

$$K_{n+1} = K_n - \xi \Delta K_n . \tag{19}$$

In the RLS algorithm (12), the loop gain ξ_n computed by (14) decreases at every iteration. A simpler method that approximates this behavior is used for the modified algorithm (19). The loop gain ξ is first set to a high value ξ_H for fast initial adjustment of the tap coefficient and then lowered to a value ξ_L to reduce fluctuations in the tap adjustment caused by noise. The modified algorithm can track variations in channel characteristics, which is not the case for the RLS algorithm given that $\xi_n \to 0$ as $n \to \infty$. The simpler method of switching the loop gain once instead of changing it according to (14) does not result in a loss of convergence speed.

Initial adjustment of the tap coefficient can be accelerated by transmitting a training sequence which consists of the repeated 18-bit long sequence:

$$\ldots +1 +1 -1 +1 +1 -1 -1 -1 -1 +1 +1 +1 +1 -1 -1 +1 -1 -1 \ldots \tag{20}$$

Transmitting this sequence leads to well decoupled adjustments of the VGA gain and tap coefficient. Correct timing phase adjustment is also maintained.

4. Structure of an Adaptive Cosine Equalizer Using the Invention

Fig.4 shows the block diagram of an adaptive cosine equalizer which consists of a basic cosine equalizer and tap coefficient adjustment means implementing the tap coefficient updating method represented by equations (18) and (19).

The ACE includes: a delay line, comprising two delay elements 27 and 29 and having two outer taps 31, 35 and a center tap 33, the first outer tap being connected to line 19 for receiving the input sample x_n; an adder 39 for combining the samples x_n at tap 31 and x_{n-2} at tap 35 to provide their sum u_n on line 41; multiplying means 43 for multiplying sample sum u_n by tap coefficient K_n; an adder 37 for adding the product $K_n u_n$ to the sample

x_{n-1} appearing at the center tap of the delay line, for generating the output sample y_n on output line 23; and a tap coefficient adjustment means 45 having two inputs connected to lines 23 and 41 for receiving y_n and u_n, and an output furnishing the tap coefficient K_n on line 47.

A digital implementation of the basic cosine equalizer will be briefly described in the next section in connection with Fig.5.

The tap coefficient adjustment means 45 which is an important part of the invented adaptive equalizer comprises the following elements in its first portion 45A (which furnishes tap coefficient gradient ΔK_n):

- a quantizer 51 connected to output line 23 for receiving output sample y_n, and furnishing on its output a reconstructed sample $\hat{z}_n$ of the nominal PR-IV sample z_n which is either 2, 0, or -2 according to (15);
- subtracting means 53 connected to receive the output sample y_n from line 23 and the reconstructed sample $\hat{z}_n$ from the output of quantizer 51, respectively, and furnishing their difference as error value $e_n(K_n)$ on its output;
- a quantizer 55 connected to line 41 for receiving the sample sum u_n of the samples x_n and x_{n-2} and furnishing on its output the reconstructed sum $\hat{u}_n$ which is a reconstruction of the sum of the nominal PR-IV samples z_n and z_{n-2}, and which is either 2, 0, or -2 according to (16);
- combining means 57 connected to the output of subtracting means 53 and of quantizer 55 for receiving $e_n(K_n)$ and $\hat{u}_n$, and furnishing at its output 59 the product of both. However, instead of an explicit multiplication, only a selection from the three values $-2e_n(K_n)$, 0 , or $+2e_n(K_n)$ need to be made because the reconstructed sum $\hat{u}_n$ is ternary.
- a delay element 61 connected to the output of combining means 57 for delaying the respective output value by one sampling period T;
- an adder 63 connected to the outputs of combining means 57 and of delay element 61, for producing at its output 65 tap coefficient gradient ΔK_n in accordance with (18).

A digital implementation of the first portion 45A of tap coefficient adjustment means 45 will be briefly described in the next section in connection with Fig.6.

Tap coefficient adjustment means 45 further comprises (as shown in the second portion 45B in Fig.4):

- multiplication means 67 for multiplying the tap coefficient gradient ΔK_n furnished on line 65, by a loop gain ξ applied to input 69. This loop gain ξ assumes first the higher and then the lower of two preselected values ξ_H (69A) and ξ_L (69B), the switchover (69C) between these two values being performed at a predetermined time. Good values for the two loop gain factors and the switchover time can be determined either by simulation or by trial operation of the circuitry. It should be noted that no explicit multiplication is required when the loop gain ξ is a multiple power of two; then the loop gain can be adjusted by changing the weight of all bits of the gradient ΔK_n (shifting).
- subtracting means 71 for forming a new equalizer tap coefficient K_n from a previous tap coefficient K_{n-1} and the weighted gradient $\xi\Delta K_{n-M}$, furnishing the new tap coefficient on line 47;
- a delay element 73 connected to line 47, for delaying the equalizer tap coefficient K_n by one sampling period and for furnishing its output K_{n-1} to subtracting means 71.

A loop delay shown at 75 in Fig.4 has been introduced in the tap adjustment means 45 to represent the inherent signal processing delay caused by the time required to compute a gradient ΔK_n and update the equalizer tap coefficient. In Fig.4 a loop delay of M sampling periods T is shown. The delay elements are of course not concentrated at one location as shown in Fig.4 but distributed as single pipeline registers at proper locations in the digital realization of means 45. The number M depends on the signaling rate 1/T and on the technology used to realize the ACE.

5. Digital Implementation of the Adaptive Cosine Equalizer

In the following, a digital implementation of the cosine equalizer and the first portion (45A) of the tap coefficient adjustment means 45 will be described. A digital realization of the second portion (45B) shown in Fig.4 is straightforward and will not be discussed.

Fig.5 shows the circuit implementation of the basic cosine equalizer. The input sample x_n is quantized with six bits and represented in two's complement (TC) form. The weight of its least significant bit (LSB) is 0.125. It should be noted that the amount of half an LSB has to be added to the sample x_n to compensate a displacement intentionally introduced by the analog-to-digital converter adjustment. In principle, this can be done at once by physically introducing a "seventh" bit with weight 2^{-4} which is always set to '1'. However, to simplify significantly the hardware design by taking advantage of this representation, the correction term is not added before some other operations are performed on the received bits. A 7-bit full adder is used to compute the sample $u_n = x_n + x_{n-2}$. At this stage the "seventh" bit with weight 2^{-4} of x_n and x_{n-2} is taken into account. The sample u_n is multiplied by the tap coefficient K_n. K_n is quantized with 4 bits and its absolute value is limited to

0.25. The product is quantized with 6 bits and sign extended before being added to the sample x_{n-1} represented in offset binary (OB) form. Element 81 converts the sample x_{n-1} appearing on line 33 from TC form to OB representation. The resulting sum is furnished in offset binary representation because a TC and OB number are added. In case of underflow or overflow the output saturates to its minimum or maximum value. The saturation circuit consists of one EXOR gate and a multiplexer. It is activated when the most significant bit (MSB) of the TC sample at the input of adder 37 does not equal the carry output c_o of the adder; in this case the carry determines the saturation value. The equalizer output sample y_n is represented in the same form as the received sample x_n.

Circuitry for a digital implementation of the first portion 45A of tap coefficient adjustment means 45 (cf. Fig.4) is shown in Fig.6. Both input samples y_n and u_n are represented in two's complement form and are provided by the cosine equalizer (cf. Fig.5) on lines 23 and 41. Relations (11), (15) and (16) show that the term $e_n\hat{u}_n/2$ can be computed as follows:

$$\frac{e_n\hat{u}_n}{2} = \begin{cases} y_n - 2 & \text{for } u_n \geq 1 \text{ and } y_n \geq 1 \\ y_n & \text{for } u_n \geq 1 \text{ and } |y_n| < 1 \\ y_n + 2 & \text{for } u_n \geq 1 \text{ and } y_n \leq -1 \\ 0 & \text{for } |u_n| < 1 \\ -y_n + 2 & \text{for } u_n \leq -1 \text{ and } y_n \geq 1 \\ -y_n & \text{for } u_n \leq -1 \text{ and } |y_n| < 1 \\ -y_n - 2 & \text{for } u_n \leq -1 \text{ and } y_n \leq -1 \end{cases} \quad (21)$$

Since its absolute value is less than or equal to 1.9375, it can be represented by five bits. Its computation using a simple EXOR/AND circuit combination is shown in portion 83 of Fig.6. This portion includes a group of five EXOR gates 83A, one additional EXOR gate 83B, and a group of five AND gates 83C. Its output signal is determined by a binary control signal B1 indicating when $u_n < 0$, by a binary control signal B2 indicating when $|u_n| \geq 1$, and by a binary control signal B3 indicating when $|y_n| \geq 1$. These binary control signals appear on lines 85, 87, and 89, respectively. Their derivation from the incoming samples is shown in portions 91 and 93 of Fig.6. Depending on the sign of u_n (represented by the signal B1 on line 85), the five EXOR gates 83A invert or keep unchanged the five least significant bits of the sample y_n. If $|y_n| \geq 1$ (as indicated by the signal B3 on line 89), either the value +2 or -2 is added to y_n by inverting the bit on line 83D with the aid of EXOR gate 83B. If $|u_n| < 1$ (as indicated by the signal B2 on line 87), the output is forced to be zero by overwriting the EXOR output signals with zeros using the group of AND gates 83C. Two succeding terms $e_n\hat{u}_n/2$ (one delayed by a delay element 95) are added in a 6-bit adder 97. Two additional gates and a delay element, as shown at 99 in Fig.6 below the full adder 97, consider the "seventh" bit with weight 0.0625 of the two successive samples to be added. The resulting sum $\Delta K_n/2$ on line 65' is fed to the tap coefficient accumulator as shown in Fig.4.

Claims

1. A method for tap coefficient adjustment in a readback equalizer of a storage system using partial-response signaling, said equalizer comprising a delay line with two outer taps and a center tap, the outer tap samples being multiplied by tap coefficient K_n, characterized by the following steps : an equalizer output sample y_n being generated by combining the multiplied outer tap samples and the center tap sample,
   - deriving a reconstructed sample $\hat{\hat{Z}}_n$ from said equalizer output sample y_n by a quantizing operation, the resulting reconstructed sample having any one of p different nominal values (e.g. +2, 0, -2);
   - deriving a reconstructed sum $\hat{u}_n$ by first adding the outer tap samples and then quantizing the resulting sample sum u_n so that the reconstructed sum $\hat{u}_n$ has any one of q different predetermined values (e.g. +2, 0, -2); and
   - combining said reconstructed sum $\hat{u}_n$, said reconstructed sample $\hat{\hat{Z}}_n$, and said output sample y_n , to generate a tap coefficient gradient ΔK_n for updating said tap coefficient K_n.

2. Tap coefficient adjustment method in accordance with Claim 1, further inluding the steps of:

- generating an error value e_n by subtracting said reconstructed sample $\hat{Z}_n$ from said output sample y_n;
- multiplying said error value e_n and said reconstructed sum $\hat{u}_n$ by combinational logic operations; and
- delaying the resulting product, and adding a delayed and current resulting product to derive tap coefficient gradient ΔK_n.

3. Tap coefficient adjustment method in accordance with Claim 1 or 2, including the further step of:
   - generating a training sequence of the form
   $$+1+1-1+1+1-1-1-1-1+1+1+1+1-1-1+1-1-1,$$
   and
   - furnishing said training sequence repeatedly to the input of said storage system prior to furnishing a data signal to it, to attain fast initial tap coefficient adjustment.

4. Tap coefficient adjustment method in accordance with Claim 1, 2 or 3, comprising the following additional steps:
   - multiplying said tap coefficient gradient ΔK_n by a loop gain factor ξ, said loop gain factor being selected from two given gain values (ξ_H, ξ_L), and
   - initially selecting the high value (ξ_H) of said two gain values for fast initial adjustment, and
   - subsequently selecting the low value (ξ_L) of said two gain values to reduce fluctuations in the tap adjustment caused by noise to derive tap coefficient K_n.

5. Tap coefficient adjustment method in accordance with Claim 4, wherein said two given gain values (ξ_H, ξ_L) are powers of 2, and wherein the multiplication of said tap coefficient gradient ΔK_n by said loop gain factor ξ is effected by a shifting operation.

6. A method for tap coefficient adjustment in a readback equalizer of a storage system using partial-response signaling, said equalizer comprising a delay line with two outer taps and a center tap, the samples appearing at the two outer taps being multiplied by a tap coefficient K_n, characterized by the following steps: an equalizer output sample y_n being generated by combining the multiplied outer tap samples and the center tap sample,
   - generating a sample sum u_n by adding the samples x_n and x_{n-2} appearing on the two outer taps;
   - deriving, from said sample sum u_n, a first binary indicator signal B1 indicating whether $u_n < 0$, and a second binary indicator signal B2 indicating whether $|u_n| \geq 1$;
   - deriving, from said output sample y_n, a third binary indicator signal B3 indicating whether $|y_n| \geq 1$;
   - combining by combinational logic operations including AND operations and EXOR operations, said output sample y_n and said first, second, and third binary indicator signals to generate a quantity A_n according to the rule

$$A_n = \begin{cases} y_n - 2 & \text{for } u_n \geq 1 \text{ and } y_n \geq 1 \\ y_n & \text{for } u_n \geq 1 \text{ and } |y_n| < 1 \\ y_n + 2 & \text{for } u_n \geq 1 \text{ and } y_n \leq -1 \\ 0 & \text{for } |u_n| < 1 \\ -y_n + 2 & \text{for } u_n \leq -1 \text{ and } y_n \geq 1 \\ -y_n & \text{for } u_n \leq -1 \text{ and } |y_n| < 1 \\ -y_n - 2 & \text{for } u_n \leq -1 \text{ and } y_n \leq -1 \end{cases};$$

and

   - adding said quantity A_n and a previously generated quantity A_{n-1} delayed by one sampling time, to obtain a tap coefficient gradient $\Delta K_n/2$ for updating said tap coefficient K_n.

7. Equalizer for executing the method of Claim 1 or 6, including:
   - delay line means (27, 29) comprising two delay elements and having a first outer tap (31) connected

to the input (19) of the equalizer, a center tap (33), and a second outer tap (35);
- first adding means (39) connected to the first (31) and second (35) outer taps, providing on its output (41) a sample sum u_n;
- multiplying means (43) connected to the output of said first adding means (39) and to a tap coefficient line (47), providing on its output an intermediate value;
- second adding means (37) connected to said center tap (33) and to the output of said multiplying means (43), its output being connected to the equalizer output line (23) for furnishing an equalizer output sample y_n; and
- tap coefficient adjustment means (45) having two inputs connected to the outputs (41, 23) of said first and second adding means (37, 39), and having an output connected to said tap coefficient line (47).

8. Equalizer apparatus in accordance with Claim 7, in which said tap coefficient adjustment means (45) includes:
- tap coefficient gradient generation means (45A) for receiving said sample sum u_n and said equalizer output sample y_n from the outputs (41, 23) of said first and second adding means, respectively, furnishing on its output (65) a tap coefficient gradient ΔK_n; and
- tap coefficient updating means (45B) being connected to said tap coefficient gradient generation means for receiving said tap coefficient gradient ΔK_n, and furnishing a tap coefficient K_n to said tap coefficient line (47).

9. Equalizer in accordance with Claim 8, wherein said tap coefficient gradient generation means (45A) comprises
- combinational logic circuitry (83, 91, 93) for generating a quantity A_n in response to said sample sum u_n and said equalizer output sample y_n
and
- delay means (95) and adding means (97) connected to the output of said combinational logic circuitry, for generating a tap coefficient gradient.

10. Equalizer in accordance with Claim 8 or 9, wherein said tap coefficient updating means (45B) comprises means (67, 69, 69A, 698) for executing multiplication operation on said tap coefficient gradient ΔK_n.

Patentansprüche

1. Verfahren zur Einstellung der Bewertungsfaktoren für die abgegriffenen Signale in einem Rückleseentzerrer eines Speichersystems, bei dem eine Partial-Response-Signalisierung verwendet wird, der Entzerrer eine Verzögerungsleitung mit zwei äußeren Abgriffen und einem Mittelabgriff umfaßt, die Abtastwerte der äußeren Abgriffe mit dem Bewertungsfaktor für das abgegriffene Signal K_n multipliziert werden, gekennzeichnet durch die folgenden Schritte:
- Erzeugen eines Entzerrerausgangswertes y_n durch Kombination der multiplizierten außen abgegriffenen Signale und des in der Mitte abgegriffenen Signals;
- Ableiten eines rekonstruierten Wertes $\hat{z}_n$ aus dem Entzerrerausgangswert y_n durch eine Quantisierungsoperation, wobei der resultierende rekonstruierte Wert einen von p unterschiedlichen Nennwerten annimmt (z.B. +2, 0, -2);
- Ableiten einer rekonstruierten Summe $\hat{u}_n$, indem zuerst die außen abgegriffenen Werte addiert werden und dann die resultierende Summe u_n so quantisiert wird, daß die rekonstruierte Summe $\hat{u}_n$ einen von q unterschiedlichen vorgegebenen Werten hat (z.B. +2, 0, -2);
- Kombinieren der rekonstruieren Summe $\hat{u}_n$, des rekonstruierten Wertes $\hat{z}_n$ und des Ausgangswertes y_n, um einen Bewertungsfaktorgradienten ΔK_n zur Aktualisierung des Bewertungsfaktors K_n für das abgegriffene Signal zu erzeugen.

2. Einstellverfahren für die Bewertungsfaktoren für die abgegriffenen Signale nach Anspruch 1, das weiterhin die folgenden Schritte umfaßt:
- Erzeugen eines Fehlerwertes e_n durch Subtraktion des rekonstruierten Wertes $\hat{z}_n$ vom Ausgangswert y_n;
- Multiplizieren des Fehlerwertes e_n und der rekonstruierten Summe $\hat{u}_n$ durch kombinatorische logische Operationen und

- Verzögern des resultierenden Produktes und Addition eines verzögerten und eines momentanen resultierenden Produktes, um daraus den Bewertungsfaktorgradienten ΔK_n abzuleiten.

3. Einstellverfahren für die Bewertungsfaktoren für die abgegriffenen Signale nach Anspruch 1 oder 2, das als weiteren Schritt umfaßt:
- Erzeugung einer Trainingsimpulsfolge der Form

$$+1+1-1+1+1-1-1-1-1+1+1+1+1-1-1+1-1-1$$

und
- wiederholtes Bereitstellen der Trainingsimpulsfolge am Eingang des Speichersystems, bevor ein Datensignal dort angelegt wird, um ein schnelles Ansprechen der Bewertungsfaktoreinstellung zu erhalten.

4. Einstellverfahren für die Bewertungsfaktoren für die abgegriffenen Signale nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß es die folgenden zusätzlichen Schritte umfaßt:
- Multiplizieren des Bewertungsfaktorgradienten ΔK_n mit einem Kreisverstärkungsfaktor ξ, wobei dieser Kreisverstärkungsfaktor aus zwei gegebenen Verstärkungswerten (ξ_H, ξ_L) ausgewählt wird und
- anfänglich der größere Wert (ξ_H) der beiden Verstärkungswerte für ein schnelles Ansprechen des Einstellvorganges ausgewählt wird und
- nachfolgend der niedrigere Wert (ξ_L) der beiden Verstärkungswerte ausgewählt wird, um Fluktuationen in der Bewertungsfaktoreinstellung aufgrund des Rauschens zu reduzieren und um den Bewertungsfaktor K_n für das abgegriffene Signal abzuleiten.

5. Einstellverfahren für die Bewertungsfaktoren für die abgegriffenen Signale nach Anspruch 4, dadurch gekennzeichnet, daß die zwei vorgegebenen Verstärkungswerte (ξ_H, ξ_L) Potenzen von 2 sind und daß die Multiplikation des Bewertungsfaktorgradienten ΔK_n mit dem Kreisverstärkungsfaktor ξ durch eine Verschiebeoperation ausgeführt wird.

6. Verfahren zur Einstellung der Bewertungsfaktoren für die abgegriffenen Signale in einem Rückleseentzerrer eines Speichersystems, bei dem eine Partial-Response-Signalisierung verwendet wird, der Entzerrer eine Verzögerungsleitung mit zwei äußeren Abgriffen und einem Mittelabgriff umfaßt, die Abtastwerte, die an den äußeren Abgriffen erscheinen, mit einem Bewertungsfaktor für das abgegriffene Signal K_n multipliziert werden, gekennzeichnet durch die folgenden Schritte:
- Erzeugen eines Entzerrerausgangswertes y_n durch Kombination der multiplizierten außen abgegriffenen Signale und des in der Mitte abgegriffenen Signals;
- Erzeugen eines Summenwertes u_n durch Addition der Abtastwerte x_n und x_{n-2}, die an den zwei äußeren Abgriffen erscheinen;
- Ableiten eines ersten binären Indikatorsignals B1, das anzeigt, ob $u_n < 0$ gilt und eines zweiten binären Indikatorsignals B2, das anzeigt, ob $|u_n| \geq 1$ gilt, aus dem Summenwert u_n;
- Ableiten eines dritten binären Indikatorsignals B3, das anzeigt, ob $|y_n| \geq 1$ gilt, aus dem Ausgangswert y_n;
- Kombinieren des Ausgangswertes y_n und des ersten, zweiten und dritten binären Indikatorsignals zur Erzeugung einer Größe A_n mittels kombinatorischer logischer Operationen, die UND-Operationen und Antivalenzoperationen umfassen, entsprechend der folgenden Regel

$$A_n = \begin{cases} y_n - 2 & \text{für } u_n \geq 1 \text{ und } y_n \geq 1 \\ y_n & \text{für } u_n \geq 1 \text{ und } |y_n| < 1 \\ y_n + 2 & \text{für } u_n \geq 1 \text{ und } y_n \leq -1 \\ 0 & \text{für } |u_n| < 1 \\ -y_n + 2 & \text{für } u_n \leq -1 \text{ und } y_n \geq 1 \\ -y_n & \text{für } u_n \leq -1 \text{ und } |y_n| < 1 \\ -y_n - 2 & \text{für } u_n \leq -1 \text{ und } y_n \leq -1 \end{cases}$$

und

- Addieren dieser Größe A_n und einer vorher erzeugten Größe A_{n-1}, die um eine Abtastperiode verzögert

ist, um einen Bewertungsfaktorgradienten $\Delta K_n/2$ zur Aktualisierung des Bewertungsfaktors K_n für das abgegriffene Signal zu erhalten.

7. Entzerrer zur Ausführung des Verfahrens nach Anspruch 1 oder 6, umfassend:
   - Verzögerungsleitungsmittel (27, 29), die zwei Verzögerungselemente umfassen und einen ersten äußeren Abgriff (31) haben, der mit dem Eingang (19) des Entzerrers verbunden ist sowie einen Mittelabgriff (33) und einen zweiten äußeren Abgriff (35);
   - erste Additionsmittel (39), die mit dem ersten (31) und dem zweiten (35) äußeren Abgriff verbunden sind und an ihrem Ausgang (41) einen Summenwert u_n bereitstellen;
   - Multiplikationsmittel (43), die mit dem Ausgang der ersten Additionsmittel (39) und mit einer Bewertungsfaktorleitung (47) verbunden sind und die an ihrem Ausgang einen Zwischenwert bereitstellen;
   - zweite Additionsmittel (37), die mit dem Mittelabgriff (33) und mit dem Ausgang der Multiplikationsmittel (43) verbunden sind und deren Ausgang mit der Entzerrerausgangsleitung (23) zur Bereitstellung des Entzerrerausgangswertes y_n verbunden ist und
   - Einstellmittel (45) für den Bewertungsfaktor für das abgegriffene Signal, die zwei Eingänge haben, welche mit den Ausgängen (41, 23) der ersten und zweiten Additionsmittel (37, 39) verbunden sind und die einen Ausgang haben, der mit der Bewertungsfaktorleitung (47) verbunden ist.

8. Entzerrervorrichtung nach Anspruch 7, dadurch gekennzeichnet, daß die Einstellmittel (45) für den Bewertungsfaktor für das abgegriffene Signal umfassen:
   - Erzeugungsmittel (45A) für einen Bewertungsfaktorgradienten zum Empfang des Summenwertes u_n und des Entzerrerausgangswertes y_n von den Ausgängen (41, 23) der ersten beziehungsweise zweiten Additionsmittel und die an ihrem Ausgang (65) einen Bewertungsfaktorgradienten ΔK_n bereitstellen und
   - Aktualisierungsmittel (45B) für den Bewertungsfaktor für das abgegriffene Signal, die mit den Erzeugungsmitteln für den Bewertungsfaktorgradienten verbunden sind, um den Bewertungsfaktorgradienten ΔK_n zu empfangen und um einen Bewertungsfaktor K_n für das abgegriffene Signal auf der Bewertungsfaktorleitung (47) bereitzustellen.

9. Entzerrer nach Anspruch 8, dadurch gekennzeichnet, daß die Erzeugungsmittel (45A) für einen Bewertungsfaktorgradienten umfassen:
   - kombinatorische logische Schaltungen (83, 91, 93) zur Erzeugung einer Größe A_n in Abhängigkeit von dem Summenwert u_n und dem Entzerrerausgangswert y_n und
   - Verzögerungsmittel (95) und Additionsmittel (97), die mit dem Ausgang der kombinatorischen logischen Schaltungen verbunden sind, um einen Bewertungsfaktorgradienten zu erzeugen.

10. Entzerrer nach Anspruch 8 oder 9, dadurch gekennzeichnet, daß die Aktualisierungsmittel (45B) für den Bewertungsfaktor für das abgegriffene Signal Mittel (67, 69, 69A, 69B) zur Ausführung von Multiplikationsoperationen mit dem Bewertungsfaktorgradienten ΔK_n umfassen.

Revendications

1. Procédé pour l'ajustement de coefficient de prise dans un égaliseur de lecture d'un système de stockage utilisant la signalisation à réponse partielle, ledit égaliseur comprenant une ligne à retard avec deux prises extérieures et une prise centrale, les échantillons des prises extérieures étant multipliés par le coefficient de prise K_n, un échantillon de sortie de l'égaliseur y_n étant produit en combinant les échantillons de prise extérieure multipliés et l'échantillon de prise centrale, caractérisé par les étapes suivantes consistant à :
   - obtenir un échantillon reconstitué $\hat{Z}_n$ à partir dudit échantillon de sortie d'égaliseur y_n par une opération de quantification, l'échantillon reconstitué obtenu présentant une valeur quelconque parmi p valeurs différentes nominales (par exemple +2, 0, -2),
   - obtenir une somme reconstituée $\hat{u}_n$ en ajoutant tout d'abord les échantillons de prise extérieure et en quantifiant ensuite la somme d'échantillon obtenu $\hat{u}_n$ de sorte que la somme reconstituée u_n présente une valeur quelconque parmi q valeurs prédéterminées différentes (par exemple +2, 0, -2), et
   - combiner ladite somme reconstituée $\hat{u}_n$, ledit échantillon reconstitué $\hat{Z}_n$ et ledit échantillon de sortie y_n afin de produire un gradient de coefficient de prise ΔK_n pour mettre à jour ledit coefficient de prise K_n.

2. Procédé d'ajustement de coefficient de prise selon la revendication 1, comportant de plus les étapes consistant à :
   - produire une valeur d'erreur e_n en soustrayant ledit échantillon reconstitué $\hat{z}_n$ dudit échantillon de sortie y_n,
   - multiplier ladite valeur d'erreur e_n et ladite somme reconstituée $\hat{u}_n$ par des opérations logiques combinatoires, et
   - retarder le produit obtenu et ajouter un produit résultant retardé et actuel afin d'obtenir le gradient de coefficient de prise ΔK_n.

3. Procédé d'ajustement de coefficient de prise selon la revendication 1 ou 2, comportant l'étape supplémentaire consistant à :
   - produire une séquence d'apprentissage sous la forme

     + 1 + 1 - 1 + 1 + 1 - 1 - 1 - 1 - 1 + 1 + 1 + 1 + 1 - 1 - 1 + 1 - 1 - 1,

     et
   - délivrer ladite séquence d'apprentissage de manière répétée à l'entrée dudit système de stockage avant de délivrer un signal de données à celui-ci afin d'atteindre un ajustement de coefficient de prise initial rapide.

4. Procédé d'ajustement de coefficient de prise selon la revendication 1, 2 ou 3, comprenant les étapes supplémentaires suivantes :
   - multiplier ledit gradient de coefficient de prise ΔK_n par un facteur de gain de boucle ξ, ledit facteur de gain de boucle étant choisi parmi deux valeurs de gain données (ξ_H, ξ_L), et
   - sélectionner initialement la valeur haute (ξ_H) desdites deux valeurs de gain pour un ajustement initial rapide, et
   - sélectionner par la suite la valeur basse (ξ_L) desdites deux valeurs de gain afin de diminuer les fluctuations de l'ajustement de prise provoquées par le bruit afin d'obtenir le coefficient de prise K_n.

5. Procédé d'ajustement de coefficient de prise selon la revendication 4, dans lequel les deux valeurs de gain données (ξ_H, ξ_L) sont des puissances de 2 et dans lequel la multiplication dudit gradient de coefficient de prise ΔK_n par ledit facteur de gain de boucle ξ est effectuée par une opération de décalage.

6. Procédé pour l'ajustement de coefficient de prise dans un égaliseur de lecture d'un système de stockage utilisant la signalisation à réponse partielle, ledit égaliseur comprenant une ligne à retard comportant deux prises extérieures et une prise centrale, les échantillons apparaissant sur les deux prises extérieures étant multipliés par un coefficient de prise K_n, un échantillon de sortie d'égaliseur y_n étant produit en combinant les échantillons de prise extérieure multipliés et l'échantillon de prise centrale, caractérisé par les étapes suivantes consistant à :
   - produire une somme d'échantillon u_n par l'addition des échantillons x_n et x_{n-2} apparaissant sur les deux prises extérieures,
   - obtenir à partir de ladite somme d'échantillon u_n un premier signal indicateur binaire B1 indiquant si $u_n < 0$ et un second signal indicateur binaire B2 indiquant si $|u_n| \geq 1$;
   - obtenir à partir dudit échantillon de sortie y_n un troisième signal indicateur binaire B3 indiquant si $|y_n| \geq 1$,
   - combiner par des opérations logiques combinatoires comportant des opérations ET et des opérations OU exclusives ledit échantillon de sortie y_n et lesdits premier, second et troisième signaux indicateurs binaires afin de produire une quantité A_n conformément à la règle

$$A_n = \begin{cases} y_n - 2 & \text{pour } u_n \geq 1 \text{ et } y_n \geq 1 \\ y_n & \text{pour } u_n \geq 1 \text{ et } |y_n| < 1 \\ y_n + 2 & \text{pour } u_n \geq 1 \text{ et } y_n \leq -1 \\ 0 & \text{pour } |u_n| < 1 \\ -y_n + 2 & \text{pour } u_n \leq -1 \text{ et } y_n \geq 1 \\ -y_n & \text{pour } u_n \leq -1 \text{ et } |y_n| < 1 \\ -y_n - 2 & \text{pour } u_n \leq -1 \text{ et } y_n \leq -1 \end{cases}$$

et

- ajouter ladite quantité A_n et une quantité précédemment produite A_{n-1} retardée d'une période d'échantillonnage afin d'obtenir un gradient de coefficient de prise $\Delta K_n/2$ pour mettre à jour ledit coefficient de prise K_n.

7. Egaliseur pour exécuter le procédé selon la revendication 1 ou 6, comportant :
   - un moyen de ligne à retard (27, 29) comprenant deux éléments à retard et comportant une première prise extérieure (31) connectée à l'entrée (19) de l'égaliseur, une prise centrale (33) et une seconde prise extérieure (35),
   - un premier moyen d'addition (39) connecté aux première (31) et seconde (35) prises extérieures, délivrant sur sa sortie (41) une somme d'échantillon u_n,
   - un moyen de multiplication (43) connecté à la sortie dudit premier moyen d'addition (39) et à une ligne de coefficient de prise (47), délivrant sur sa sortie une valeur intermédiaire,
   - un second moyen d'addition (37) connecté à ladite prise centrale (33) et à la sortie dudit moyen de multiplication (43), sa sortie étant connectée à la ligne de sortie d'égaliseur (23) pour délivrer un échantillon de sortie d'égaliseur y_n, et
   - un moyen d'ajustement de coefficient de prise (45) comportant deux entrées connectées aux sorties (41, 23) des premier et second moyens d'addition (37, 39) et comprenant une sortie connectée à ladite ligne de coefficient de prise (47).

8. Dispositif égaliseur selon la revendication 7, dans lequel ledit moyen d'ajustement de coefficient de prise (45) comporte :
   - un moyen de génération de gradient de coefficient de prise (45A) pour recevoir ladite somme d'échantillon u_n et ledit échantillon de sortie d'égaliseur y_n à partir des sorties (41, 23) desdits premier et second moyens d'addition, respectivement, délivrant sur sa sortie (65) un gradient de coefficient de prise ΔK_n, et
   - un moyen de mise à jour de coefficient de prise (45B) qui est connecté audit moyen de génération de gradient de coefficient de prise pour recevoir ledit gradient de coefficient de prise K_n et fournir un coefficient de prise ΔK_n sur ladite ligne de coefficient de prise (47).

9. Egaliseur selon la revendication 8, dans lequel ledit moyen de génération de gradient de coefficient de prise (45A) comprend :
   - des circuits logiques combinatoires (83, 91, 93) pour produire une quantité A_n en réponse à ladite somme d'échantillon u_n et à audit échantillon de sortie d'égaliseur y_n, et
   - un moyen de retard (95) et un moyen d'addition (97) connectés à la sortie desdits circuits logiques combinatoires pour produire un gradient de coefficient de prise.

10. Egaliseur selon la revendication 8 ou 9, dans lequel le moyen de mise à jour de coefficient de prise (45B) comprend des moyens (67, 69, 69A, 69B) pour exécuter les opérations de multiplication sur ledit gradient de coefficient de prise K_n.

FIG. 1

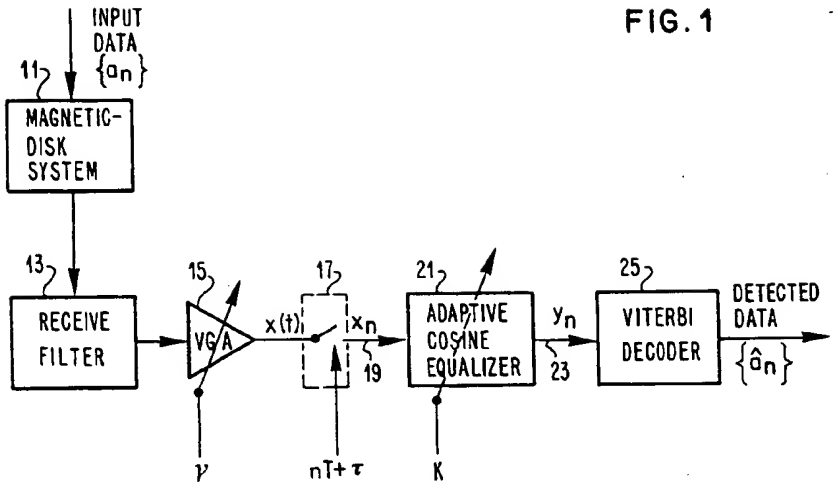
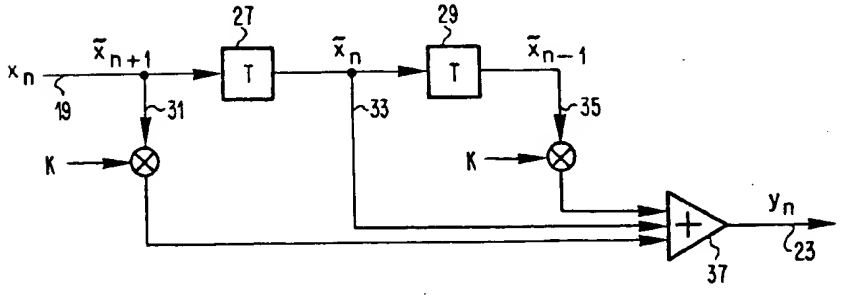

INPUT DATA
{an}
11
MAGNETIC-DISK SYSTEM
13
RECEIVE FILTER
15
VGA
x(t)
17
xn
19
21
ADAPTIVE COSINE EQUALIZER
yn
23
25
VITERBI DECODER
DETECTED DATA
{ân}
γ
nT+τ
K

FIG. 2


xn
19
x̃n+1
31
27
T
x̃n
33
29
T
x̃n-1
35
K
K
yn
23
37

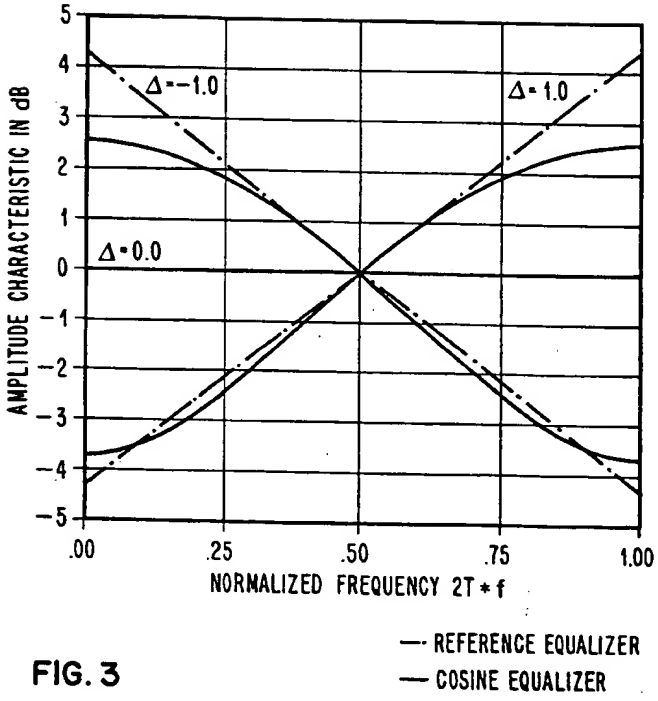

AMPLITUDE CHARACTERISTIC IN dB
5
4
3
2
1
0
−1
−2
−3
−4
−5
Δ=−1.0
Δ=1.0
Δ=0.0
.00
.25
.50
.75
1.00
NORMALIZED FREQUENCY 2T * f
— REFERENCE EQUALIZER
— COSINE EQUALIZER

FIG. 3

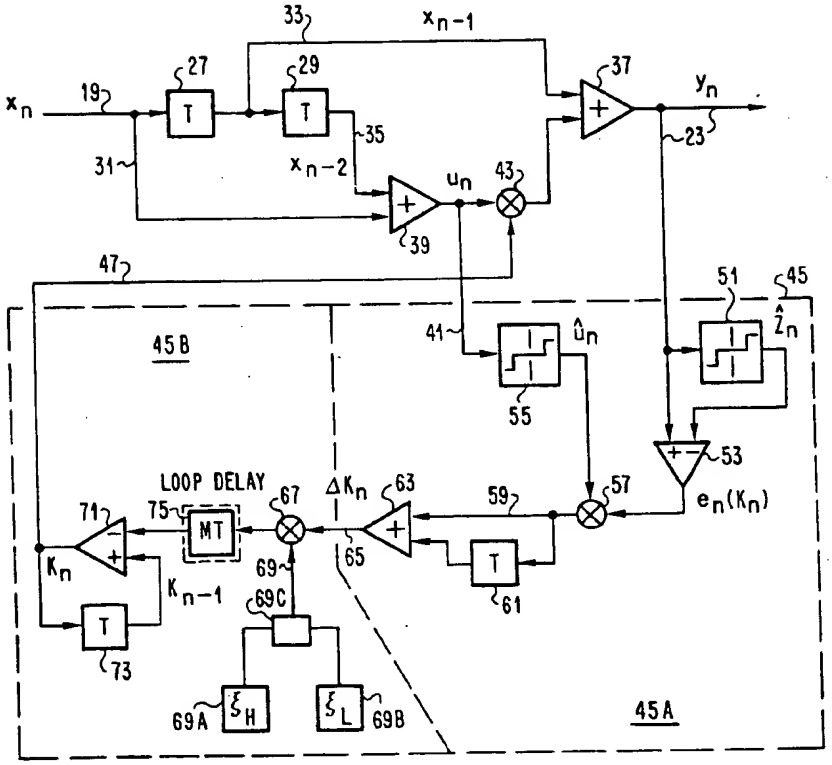

33
x_{n-1}
x_n
19
27
T
29
T
35
37
y_n
23
31
x_{n-2}
u_n
43
39
47
51
45
$\hat{z}_n$
45B
41
$\hat{u}_n$
55
53
$e_n(K_n)$
LOOP DELAY
67
ΔK_n
63
59
57
71
75
MT
K_n
69
65
T
61
K_{n-1}
69C
T
73
69A
ξ_H
ξ_L
69B
45A

FIG. 4

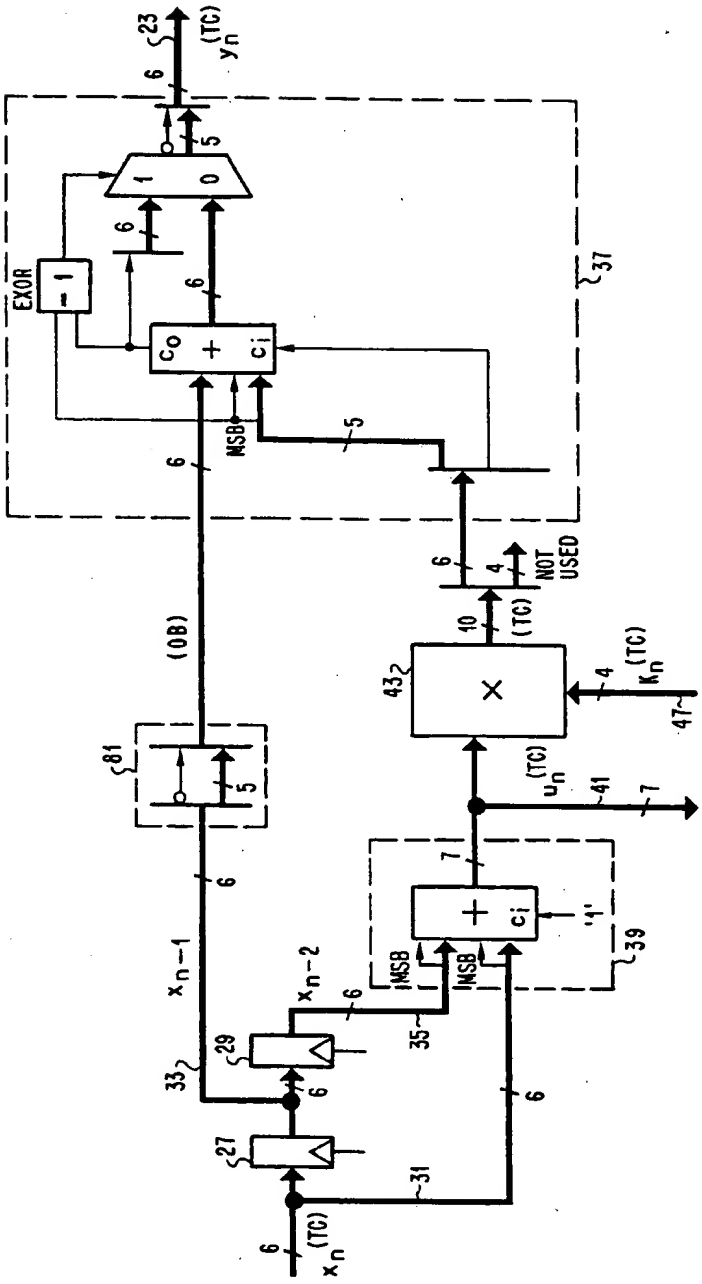

23
6
y_n (TC)
5
1
0
6
6
EXOR
-1
c_o
+
c_i
37
NSB
5
6
6
4
NOT USED
10
(TC)
43
×
4
K_n (TC)
47
(OB)
81
5
6
u_n (TC)
41
7
7
+
c_i
'1'
39
x_{n-1}
x_{n-2}
6
MSB
MSB
35
33
29
6
6
27
31
6
6
x_n (TC)
17

FIG. 5

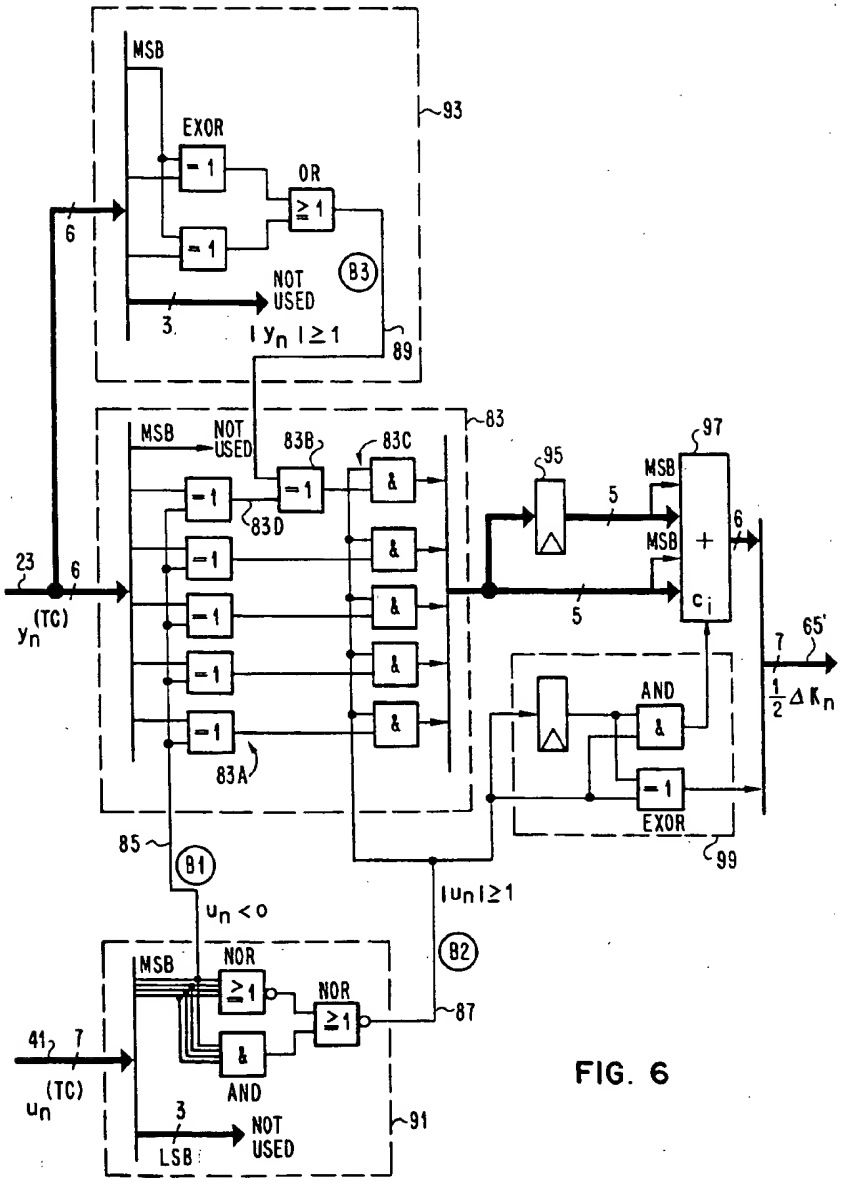

MSB
EXOR
OR
NOT USED
93
89
83
MSB
NOT USED
83B
83C
83D
83A
95
97
MSB
MSB
AND
EXOR
99
65'
85
B1
B2
B3
87
91
NOR
NOR
AND
NOT USED
LSB
(TC)
(TC)

FIG. 6